<Title>

ANALOG-TO-DIGITAL CONVERSION CIRCUIT AND IMAGE PROCESSING

CIRCUIT FOR STEPWISE CONVERSION OF A SIGNAL THROUGH MULTIPLE

STAGES OF CONVERSION UNITS

5   <BACKGROUND OF THE INVENTION>

<1.Field of the Invention>

The present invention relates to an analog-to-digital

conversion circuit, and more particularly to a technique for

reducing power consumption in the analog-to-digital conversion

10   circuit.

<2.Description of the Related Art>

Recently, cellular phones have been provided with various

additional functions such as an image shooting function, an

image reproducing function, a moving image shooting function,

15   and a moving image reproducing function. Accordingly, there

are increasing needs for an analog-to-digital converter

(hereinafter referred to as an "AD converter") incorporated

into the cellular phone to operate at lower voltages with

lower power consumption. In particular, one-chip LSIs

20   incorporating an AD converter has employed finer design rules

year by year, and thus required lower supply voltages. As an

AD converter having high conversion accuracy, known to those

skilled in the art is a multi-stage pipelined AD converter

(for example, see Japanese Patent Laid-Open Publication No.

25   Hei 9-69776, its entirety and Fig. 1).

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Reducing the overall voltage range for an analog signal to realize lower power consumption would readily cause degradation in conversion accuracy due to decreases in S/N ratio. In general, the pipelined AD converter incorporates a

5 sampling circuit with capacitors, and its mean square voltage of thermal noises is expressed by the following equation:

[Equation 1]

$$\overline{v^2} \propto kT/C$$

Assuming that the amount of thermal noise is constant as

10 expressed by Equation 1, a reduction in voltage range for an analog signal would cause a corresponding decrease in S/N ratio. For example, an overall accuracy of 10 bits would require an S/N ratio of about 60dB or more. To compensate the aforementioned S/N ratio when the voltage range is reduced, it

15 is found from Equation 1 that C has to be increased to thereby reduce the thermal noise. For example, halving the voltage range for an analog signal would make it necessary to increase C by four times to compensate for the halving. This causes an increase in size of the capacitor leading to an increase in

20 circuit area. On the other hand, uncompensated noises themselves would cause degradation in characteristics.

<SUMMARY OF THE INVENTION>

The present invention has been achieved in view of the

25 foregoing circumstances. It is therefore an object of the

present invention to provide an AD converter which operates
with lower power consumption. It is another object of the
invention to provide an AD converter which operates with lower
power consumption while avoiding an increase in circuit area
5   and deterioration in characteristics. It is still another
object of the invention to provide an AD converter which
employs a simple structure to provide improved characteristics.

One of the aspects of the present invention is an analog-
to-digital conversion circuit. This circuit comprises a group
10 of conversion units including at least two stages of
conversion units each of which produces a digital value of
several bits in stages according to an input analog voltage,
and a plurality of power sources which supply voltages to the
group of conversion units. In the group of conversion units, a
15 first stage converts a predetermined number of bits from the
most significant bit, and second and subsequent stages convert
lower-order bits than the predetermined number of bits. The
plurality of power sources supply voltages to the conversion
units in the second and subsequent stages, the voltages being
20 lower than the voltage supplied to the conversion unit in the
first stage.

In the group of conversion units, the conversion unit in
the first stage requires the highest resolution (S/N), whereas
the second and subsequent stages require gradually reduced
25 resolutions. Thus, according to this aspect, a high voltage is

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supplied only to the first stage while lower voltages are supplied to the second and subsequent stages, thereby reducing the overall voltage. As used herein, the expression "the second and subsequent stages" does not necessarily mean that

5   three or more stages of conversion units are included, but also refers to only the second stage in a group of two stages of conversion units.

Another aspect of the present invention is also an analog-to-digital conversion circuit. This circuit has a group

10   of conversion units including at least two stages of conversion units each of which produces a digital value of several bits in stages according to an input analog voltage, and a power source which supplies a voltage to the group of conversion units. In the group of conversion units, a first

15   stage converts a predetermined number of bits from the most significant bit, and second and subsequent stages convert lower-order bits than the predetermined number of bits. In the group of conversion units, a voltage supplied to a stage by the power source is lower than that supplied to its preceding

20   stage.

As described above, in the group of conversion units, the second and subsequent stages need gradually lowered resolutions. Accordingly, this aspect of the invention allows a voltage supplied to a stage to be lower than that supplied

25   to its preceding stage in the first to the subsequent stages,

thereby reducing the overall voltage.

Still another aspect of the present invention is also an analog-to-digital conversion circuit. This circuit has a group of conversion units including at least two stages of

5   conversion units each of which produces a digital value of several bits in stages according to an input analog voltage, a power source which supplies a voltage to the group of conversion units, and a voltage step-up unit which steps up the voltage. In the group of conversion units, a first stage

10   converts a predetermined number of bits from the most significant bit, and second and subsequent stages convert lower-order bits than the predetermined number of bits. The step-up unit steps up the voltage to be supplied from the power source to at least part of the conversion unit in the

15   first stage into a higher voltage.

As described above, in the group of conversion units, the second and subsequent stages need gradually lowered resolutions. Accordingly, this aspect of the invention allows a lower voltage to be supplied to other than the first stage

20   while allowing a stepped-up higher voltage to be supplied only to the first stage, thereby reducing the overall voltage while maintaining the resolution of the first stage.

In the group of conversion units, a conversion unit to which the power source supplies a lower voltage may be

25   designed to have a lower voltage range for an analog signal.

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That is, the voltage range is set corresponding to the voltage supplied to each stage, thereby reducing the overall voltage.

It is to be understood that any combinations of the foregoing components, and the components and expressions of the present invention having their methods, apparatuses, systems, and the like replaced mutually are also intended to constitute applicable aspects of the present invention.

<BRIEF DESCRIPTION OF THE DRAWINGS>

Fig. 1 is a diagram showing the basic configuration of an image processing circuit;

Fig. 2 is a diagram showing the configuration of an AD converter according to a first embodiment of the present invention;

Fig. 3 is a diagram showing the configuration of an AD converter according to a second embodiment;

Fig. 4 is a diagram showing the configuration of an AD converter according to a third embodiment;

Fig. 5 is a diagram showing the configuration of an AD converter according to a fourth embodiment; and

Fig. 6 is a diagram showing the configuration of an AD converter according to a fifth embodiment.

<DETAILED DESCRIPTION OF THE INVENTION>

(First embodiment)

Fig. 1 shows the basic configuration of an image

processing circuit. An image sensor 12 such as CCD (Charge

Coupled Device) and a CMOS sensor receives light from a

subject to convert the light into an electric signal, which is

5   then supplied to a one-chip LSI (Large Scale Integration) 10.

The one-chip LSI 10 incorporates an AGC (Auto Gain Control) 14,

an AD converter 20, and a DSP (Digital Signal Processor) 16.

The AGC 14 amplifies the electric signal received from the

image sensor 12, and the AD converter 20 converts the

10   amplified analog signal into a digital signal, on which the

DSP 16 performs compression or other image processing. Part of

the output from the DSP 16 is fed back to the AGC 14 via a

feedback circuit 18.

The one-chip LSI 10 is supplied with power from two

15   sources, i.e., a first voltage source VDD1 and a second

voltage source VDD2. The first voltage source VDD1 supplies

2.7V and the second voltage source VDD2 supplies 1.2V. Thus,

the AGC 14 is supplied with a voltage of 2.7V from the first

voltage source VDD1 while the DSP 16 is supplied with a

20   voltage of 1.2V from the second voltage source VDD2.

Conventionally, the AD converter 20 is supplied only with a

voltage of 2.7V from the first voltage source VDD1. However,

in this embodiment, the AD converter 20 is supplied with 2.7V

and 1.2V from the first and second voltage sources VDD1 and

25   VDD2, respectively.

As described later, the AD converter 20 operates at a lower voltage with lower power consumption. Accordingly, the one-chip LSI 10 and the image sensor 12 can be well incorporated into a portable terminal such as a cellular phone

5   which is highly required to operate at lower voltages. Furthermore, the AD converter 20 will not cause an increase in circuit area due to an increase in capacitance of a capacitor, thus being well incorporated into the one-chip LSI 10.

Fig. 2 illustrates the configuration of the AD converter

10   20 according to the first embodiment. The AD converter 20 includes n stages of conversion units, i.e., the first conversion unit 22 to the nth conversion unit 28, to perform 10-bit AD conversion in stages. The first stage or the first conversion unit 22 processes four bits, and the second and

15   subsequent stages process the remaining bits. For n = 4, the second to the fourth stages may each process two bits. The first stage or the first conversion unit 22 requires an accuracy of 10 bits, whereas the second stage or the second conversion unit 24 requires an accuracy of only $10 - 4 + 1 = 7$

20   bits. As such, bit accuracies required are different between the first stage and the second and subsequent stages, with different analog accuracies required, thereby resulting in voltage values essentially required being different between the first stage and the second and subsequent stages.

25   The first conversion unit 22 includes a first AD

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conversion circuit 32, a first DA conversion circuit 34, a

first subtractor circuit 36, and a first amplifier circuit 38.

The first AD conversion circuit 32 is a sub-AD conversion

circuit which converts an input analog signal into a digital

5   signal of a predetermined number of bits from the most

significant bit. For example, in this embodiment, a digital

value of four bits is delivered to the first DA conversion

circuit 34 and a digital output circuit 30. The first DA

conversion circuit 34 converts the digital value delivered

10   from the first AD conversion circuit 32 into an analog signal.

The first subtractor circuit 36 supplies the difference

between the original input analog signal and the analog signal

from the first DA conversion circuit 34 to the first amplifier

circuit 38, which then amplifies the difference to output the

15   resulting signal to the second conversion unit 24. The first

subtractor circuit 36 and the first amplifier circuit 38 may

be combined to form a differential amplifier circuit.

     The second conversion unit 24 includes a second AD

conversion circuit 42, a second DA conversion circuit 44, a

20   second subtractor circuit 46, and a second amplifier circuit

48. Each of these components operates in the same manner as

the first AD conversion circuit 32, the first DA conversion

circuit 34, the first subtractor circuit 36, and the first

amplifier circuit 38 of the first conversion unit 22,

25   respectively. However, for example, the second AD conversion

circuit 42 outputs two lower-order bits than the output bits from the first AD conversion circuit 32.

An (n-1)th conversion unit 26 includes an (n-1)th AD conversion circuit 52, an (n-1)th DA conversion circuit 54, an (n-1)th subtractor circuit 56, and an (n-1)th amplifier circuit 58. Each of these components also operates in the same manner as the first AD conversion circuit 32, the first DA conversion circuit 34, the first subtractor circuit 36, and the first amplifier circuit 38 of the first conversion unit 22, respectively. However, the (n-1)th AD conversion circuit 52 outputs two lower-order bits than the output bits from the preceding stage. The nth conversion unit 28 includes an nth AD conversion circuit 60. The nth AD conversion circuit 60 outputs the two bits or the least and second least significant bits. The digital output circuit 30 combines digital signals received from the first conversion unit 22, the second conversion unit 24, the (n-1)th conversion unit 26, and the nth conversion unit 28 to output a 10-bit digital signal.

In this embodiment, the first stage or the first conversion unit 22 needs the highest analog accuracy, and is thus supplied with a voltage of 2.7V from the first voltage source VDD1. Each of the conversion units in the second and subsequent stages or the second conversion unit 24 to the nth conversion unit 28 needs a less analog accuracy than the first conversion unit 22, and is thus supplied with a voltage of

1.2V from the second voltage source VDD2. This serves to reduce the overall power consumption when compared with a conventional case in which a voltage of about 2.7V is generally supplied. In particular, since the second voltage

5   source VDD2 is originally provided to supply a low voltage to the DSP 16 of Fig. 1 and not additionally provided to implement the AD converter 20 of this embodiment, no demerit is found in the entire system.

     The voltage supplied to the second and subsequent stages

10   is lower than that supplied to the first stage. The voltage range for an analog signal in the conversion units of the second and subsequent stages is accordingly reduced to a lower voltage value. Conventionally, for example, the numbers of bits were assigned as 4, 2, 2, and 2 to be processed in the

15   first and the subsequent stages, with the first stage being set at a corresponding voltage full-scale range of 1Vpp (peak to peak voltage) and the second stage at a voltage range of 0.5Vpp. This resulted from the numbers of bits that were assigned to maximize the processing speed of the overall AD

20   converter. In this embodiment, the voltage supplied to the second and subsequent stages is lower than that to the first stage, and the voltage range of the second and subsequent stages is reduced correspondingly. This allows, for example, the voltage range of the second and subsequent stages to be

25   reduced to a voltage of 0.25Vpp in peak value.

(Second Embodiment)

Fig. 3 shows the configuration of an AD converter 20 according to a second embodiment. The AD converter 20 according to this embodiment is different from that of the first embodiment in that voltages to be supplied to each of multiple stages of conversion units are gradually lowered. Now, the different point will be mainly described below.

The first conversion unit 22 and the second conversion unit 24 are supplied with a voltage from the first voltage source VDD1 and a voltage from the second voltage source VDD2, respectively. On the other hand, the (n-1)th conversion unit 26 and the nth conversion unit 28 are supplied with a voltage from a third voltage source VDD3 and a voltage from a fourth voltage source VDD4, respectively. The first voltage source VDD1 supplies the highest voltage, while the second voltage source VDD2 supplies the second highest voltage, the third voltage source VDD3 the third highest voltage, and the fourth voltage source VDD4 the fourth highest voltage. In this manner, the respective voltages supplied to each of the n stages of pipelined AD converters are successively lowered in n stages, thereby reducing the overall power consumption. Furthermore, the voltage ranges for an analog signal in each stage are successively reduced corresponding to the respective voltages supplied to each stage separately in n stages.

(Third Embodiment)

Fig. 4 shows the configuration of an AD converter 20

according to a third embodiment. The AD converter 20 according

to this embodiment is different from that of the first and

second embodiments in that the second voltage source VDD2

5   supplies a voltage to all of multiple stages of conversion

units. Now, the different point will be mainly described below.

The AD converter 20 has a voltage step-up unit 82 for

stepping up the voltage supplied. The step-up unit 82 steps up

the voltage, supplied by the second voltage source VDD2 to the

10   first conversion unit 22, from 1.2V to 2.7V. For example, the

step-up unit 82 includes a charge pumping DC-DC converter. In

this manner, a higher voltage is supplied only to the first

stage or the first conversion unit 22, while a lower voltage

is supplied to the second and subsequent stages or the second

15   conversion unit 24 to the nth conversion unit 28, thereby

reducing the overall voltage. Correspondingly, as in the first

embodiment, the voltage range for an analog signal of the

second and subsequent stages or the second conversion unit 24

to the nth conversion unit 28 is lowered with respect to that

20   of the first stage or the first conversion unit 22. On the

other hand, the step-up unit 82 may not only step up a voltage

supplied to the entire first conversion unit 22 but also step

up only a voltage supplied to a component included in the

first conversion unit 22. For example, the step-up unit 82 may

25   step up a voltage supplied to the first amplifier circuit 38

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included in the first conversion unit 22.

(Fourth Embodiment)

Fig. 5 shows the configuration of an AD converter 20 according to a fourth embodiment. The AD converter 20 according to this embodiment is different from that of the other embodiments in that the second voltage source VDD2 supplies a voltage to all the multiple stages of conversion units but the first voltage source VDD1 supplies a voltage only to some of the circuits of the first conversion unit 22. Now, the different point will be mainly described below.

The first conversion unit 22 further includes a sample and hold circuit 70 in addition to the first A-D conversion circuit 32, the first DA conversion circuit 34, the first subtraction circuit 36, and the first amplification circuit 38. The sample and hold circuit 70 holds an input analog signal Vin until the first subtraction circuit 36 performs a subtraction at least on the output from the first DA conversion circuit 34.

In this embodiment, the sample and hold circuit 70 included in the first stage or the first conversion unit 22 needs the highest analog accuracy, and is thus supplied with a voltage of 2.7V by the first voltage source VDD1. The other circuits included in the first conversion unit 22 needs less analog accuracy than the sample and hold circuit 70, and is thus supplied with a voltage of 1.2V by the second voltage

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source VDD2. This serves to reduce the overall power
consumption when compared with a conventional case in which a
voltage of about 2.7V is supplied to all the stages.

(Fifth Embodiment)

5   Fig. 6 shows the configuration of an AD converter 20
according to a fifth embodiment. The AD converter 20 according
to this embodiment is different from that of the fourth
embodiment in that the second voltage source VDD2 supplies a
voltage to all the multiple stages of conversion units, but is

10   similar thereto in that the first voltage source VDD1 supplies
a voltage only to some of the circuits of the first conversion
unit 22. However, the first conversion unit 22 of this
embodiment is different in configuration from the first
conversion unit 22 according to the fourth embodiment. Now,

15   the different point will be mainly described below.

The first conversion unit 22 further includes an analog
switch 72, a first sample and hold circuit 74, a second sample
and hold circuit 76, a third sample and hold circuit 78, and a
fourth sample and hold circuit 80 in addition to the first AD

20   conversion circuit 32, the first DA conversion circuit 34, the
first subtraction circuit 36, and the first amplification
circuit 38. The first sample and hold circuit 74 holds a first
input analog signal Vin1. Likewise, the second sample and hold
circuit 76 holds a second input analog signal Vin2, the third

25   sample and hold circuit 78 holds a third input analog signal

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Vin3, and the fourth sample and hold circuit 80 holds a fourth input analog signal Vin4.

The analog switch 72 selectively delivers the respective outputs from the first sample and hold circuit 74, the second
5 sample and hold circuit 76, the third sample and hold circuit 78, and the fourth sample and hold circuit 80 in that order to the first AD conversion circuit 32 and the first subtraction circuit 36. That is, the circuits downstream of the analog switch 72 sequentially AD convert the first input analog
10 signal Vin1, the second input analog signal Vin2, the third input analog signal Vin3, and the fourth input analog signal Vin4.

The first sample and hold circuit 74, the second sample and hold circuit 76, the third sample and hold circuit 78, and
15 the fourth sample and hold circuit 80 operate on a 2MHz clock. In contrast to this, the other components of the first conversion unit 22 such as the analog switch 72, the first AD conversion circuit 32, the first DA conversion circuit 34, the first subtraction circuit 36, and the first amplification
20 circuit 38, and the other components other than the first conversion unit 22 such as the second conversion portion 24, the conversion portion 26, and the nth conversion portion 28 operate on a 8MHz clock. That is, the components downstream of the analog switch 72 operate four times faster than each of
25 the sample and hold circuits. Accordingly, as a whole, four

analog values can be converted to digital values on each clock of the sample and hold circuits.

In this embodiment, the first sample and hold circuit 74, the second sample and hold circuit 76, the third sample and

5   hold circuit 78, and the fourth sample and hold circuit 80, which are included in the first stage or the first conversion unit 22, need the highest analog accuracy, and are thus supplied with a voltage of 2.7V by the first voltage source VDD1. The other circuits included in the first conversion unit

10   22 and the circuits downstream of the second conversion portion 24 need less analog accuracy than the first sample and hold circuit 74, the second sample and hold circuit 76, the third sample and hold circuit 78, and the fourth sample and hold circuit 80, and are thus supplied with a voltage of 1.8V

15   by the second voltage source VDD2. This serves to reduce the overall power consumption when compared with a conventional case in which a voltage of about 2.7V is supplied to all the stages.

Up to this point, the present invention has been

20   described in conjunction with the embodiments. These embodiments are given solely by way of illustration. It will be understood by those skilled in the art that various modified examples may be made of combinations of the foregoing components and processes, and all such modified examples are

25   also intended to fall within the scope of the present

invention. The following provides some of the modified
examples.

In each of the embodiments, the first voltage source VDD1
and the second voltage source VDD2 each supply the voltage
5   having the same value to each conversion unit of each stage in
the first conversion unit 22 to the nth conversion unit 28. In
a modified example, voltages having different values may also
be supplied to components such as the amplifiers or switches
included in the conversion unit of each stage. For example, a
10   higher voltage of 2.7V may be supplied only to a single
component included in the first stage or the first conversion
unit 22 while a lower voltage of 1.2V may be supplied to the
other components and the second and subsequent stages or the
second conversion unit 24 to the nth conversion unit 28.

15   In the third embodiment, a stepped-up voltage is provided
only to the first stage or the first conversion unit 22. In a
modified example, a plurality of step-up units may be provided
such that each unit supplies a voltage having a different
value to the conversion unit in the respective stages.

20   Alternatively, a stepped-up voltage may be supplied only to a
conversion unit that requires a higher supply voltage or to a
circuit unit in the conversion unit. This makes it possible to
supply gradually reduced voltages to the first and subsequent
stages, thereby reducing the overall voltage.

25   In each of the embodiments, an AD converter which

includes conversion units in four stages or more is shown as one example. In a modified example, an AD converter which includes conversion units in two stages or three stages may be used.

5   The second embodiment has been illustrated which has four voltage sources for supplying voltages having four values. In a modified example, a plurality of voltage sources for supplying voltages having three values or five or more values may be used. Furthermore, as another modified example,

10   voltages having a plurality of values by dividing a single voltage source with load resistors may be supplied.